Electronic Version
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Claims

[c1] 1. A multi-chip package module, comprising:
a first chip having an active surface;
a second chip positioned over the active surface of the first chip as a flip -chip structure, wherein a height of the second chip in a direction perpendicular to the active surface is defined as h1;
a plurality of first bumps positioned between the active surface of the first chip and the second chip, wherein a height of the first bumps in the direction perpendicular to the active surface is defined as h2; and
a plurality of contacts, protruding from the active surface of the first chip, wherein a height of the contacts in the direction perpendicular to the active surface is defined as h3, and values of h1, h2, and h3 are related by an in-equality of $h3 \geq h1 + h2$.

[c2] 2. The multi-chip package module of claim 1, wherein each contact comprises a plurality of stacked second bumps.

[c3] 3. The multi-chip package module of claim 1, wherein each of the contacts comprises a cylindrical metallic rod.

[c4] 4. The multi-chip package module of claim 1, further comprising an insulating material over the active surface of the first chip that encloses the first bumps and the contacts.

[c5] 5. The multi-chip package module of claim 1, wherein a portion of the second chip extends over an area outside the active surface of the first chip.

[c6] 6. The multi-chip package module of claim 1, further comprising a third chip and a plurality of third bumps, wherein the third chip is positioned over the active surface of the first chip as a flip chip structure, the third bumps are positioned between the active surface of the first chip and the third chip, a height of the third chip in the direction perpendicular to the active surface being defined as h4, a height of the third bumps in the direction perpendicular to the active surface being defined as h5, and values of h3, h4 and h5 are related by an inequality of $h3 \geq h4 + h5$.

[c7] 7. A multi-chip package structure, comprising:
a substrate;
a plurality of contacts;
a first chip having an active surface that faces the substrate, wherein the contacts are positioned between the first chip and the substrate, and a distance between the

substrate and the active surface in a direction perpendicular to the active surface is defined as d;
a second chip positioned between the first chip and the substrate, wherein a height of the second chip in the direction perpendicular to the active surface is defined as h1; and
a plurality of first bumps positioned between the active surface of the first chip and the second chip for electric connection, wherein a height of the first bumps in the direction perpendicular to the active surface is defined as h2 and values of h1, h2 and d are related by an inequality of $d \geq h1 + h2$.

[c8] 8. The multi-chip package structure of claim 7, wherein each of the contacts comprises a plurality of stacked second bumps.

[c9] 9. The multi-chip package structure of claim 7, wherein each of the contacts comprises a cylindrical metallic rod.

[c10] 10. The multi-chip package structure of claim 7, further comprising an insulating material over the active surface of the first chip that encloses the first bumps and the contacts.

[c11] 11. The multi-chip package structure of claim 7, wherein a portion of the second chip extends over an area out-

side the active surface of the first chip.

[c12] 12. The multi-chip package structure of claim 7, wherein a height of the contacts in the direction perpendicular to the active surface is defined as h3 and values of h1, h2 and h3 are related by an inequality of $h3 \geq h1 + h2$.

[c13] 13. The multi-chip package structure of claim 7, further comprising a third chip and a plurality of third bumps such that the third chip is positioned between the first chip and the substrate, as well as the third bumps are positioned between the first chip and the third chip to connect together as a flip chip structure, wherein a height of the third chip in the direction perpendicular to the active surface is defined as h4 and a height of the third bumps in the direction perpendicular to the active surface is defined as h5, and values of d, h4 and h5 are related by an inequality of $d \geq h4 + h5$.

[c14] 14. The multi-chip package structure of claim 13, wherein a height of the contacts in the direction perpendicular to the active surface is defined as h3 and values of h3, h4 and h5 are related by an inequality of $h3 \geq h4 + h5$.

[c15] 15. A multi-chip package structure, comprising:
a substrate;

a plurality of contacts;

a first chip having an active surface that faces the substrate, wherein the contacts are positioned between the first chip and the substrate to connect the first chip and the substrate as a flip chip structure, and a distance between the substrate and the active surface in the direction perpendicular to the active surface is defined as d; and

at least a package module, set up between the first chip and the substrate, and connected to the first chip, wherein the package module comprises at least a chip and a height of the package module in the direction perpendicular to the active surface is defined as h1, and values of d and h1 are related by an inequality of $d \geq h1$.

[c16] 16. The multi-chip package structure of claim 15, wherein each of the contacts comprises a plurality of stacked bumps.

[c17] 17. The multi-chip package structure of claim 15, wherein each of the contacts comprises a cylindrical metallic rod.

[c18] 18. The multi-chip package structure of claim 15, wherein the package module is an electrically-testable package module.

[c19] 19. The multi-chip package structure of claim 15, wherein the package module comprises a multi-chip module (MCM).

[c20] 20. The multi-chip package structure of claim 15, wherein the package module comprises a system in a package (SIP).

[c21] 21. The multi-chip package structure of claim 15, wherein a portion of the package module extends over an area outside the active surface of the first chip.

[c22] 22. The multi-chip package structure of claim 15, wherein the package module comprises a chip scale package (CSP).

[c23] 23. The multi-chip package structure of claim 15, wherein a height of the contacts in the direction perpendicular to the active surface is defined as h3 and the values of h1 and h3 are related by an inequality of $h3 \geq h1$.